AMENDMENTS TO THE SPECIFICATION

Please amend paragraph **[0069]** of the specification as follows.

[0069] The semiconductor memory device 100 may further include a reset control circuit 270, an address register 280 and a comparative circuit 290. The reset control circuit 270, address register 280 and comparative circuit 290 may constitute a read protection unit, such as unit 200 shown in Fig. 1. The reset control circuit 270 detects whether or not a reset command (RST_CMD) is input. If the reset command (RST_CMD) is input, the reset control circuit 270 activates the initialization signal (nRESET). A program register 359 is set to have a value of the full burst length according to the activation of the initialization signal (nRESET). A refresh control ~~signal~~ circuit 353 generates a row address such that the word lines (WL0-WLm) are sequentially activated in a similar manner as in the self-refresh mode according to the activation of the initialization signal (nRESET). Further, the refresh control circuit 353 generates a row address such that the word lines (WL0-WLm) are sequentially activated when the self-refresh command (SR_CMD) is input.